US-PAT-NO: 4998244
DOCUMENT-IDENTIFIER: US 4998244 A
TITLE: High speed module interconnection bus

Detailed Description Text - DETX (5):

In the protocol of the present invention, a reservation time slot is utilized for making bus reservations for each transmission cycle (For purposes of this document, the term "transmission cycle" is intended to mean a complete cycle as will be described comprising a reservation signal, a reservation time slot and a group of transmitted cells.). This reservation time slot is signaled by three consecutive ones on the reserve line 60. Using three consecutive ones to signal reservation eliminates the need for a master station which provides great advantages in high availability systems since all modules may power up and initialize independently.

Detailed Description Text - DETX (19):

Thus, the current protocol provides an inherent level of protection against module failure disrupting communication among other modules. At this point, when the error is detected a new module may be plugged into the slot for module 13 without powering down the entire system. The new module simply waits for the next occurrence of three consecutive ones on the reserve line 60 and begins normal operation without any sort of startup procedure needed in general. In the worst case, multiple consecutive module failures force the bus to reenter the reservation mode.

Detailed Description Text - DETX (22):

During the reservation slot of T20, no modules request transmission time. This condition illustrates the idle pattern of the reserve line 60 which takes the following form:

Detailed Description Text - DETX (29):

Referring to FIG. 5, the process begins at step 100 with power-up and initialization of the module. At decision block 102, the module determines if it has a cell to transmit. If not, the process waits at step 102 until it does. If it does have a cell to transmit, control passes to decision block 104 where the module waits for three consecutive ones to appear on the reserve line 60. When they appear, the module (module N) pulls line N of the data/reservation bus to a logic zero at step 106.

Detailed Description Text - DETX (44):

Turning now to FIG. 9, the transmit block 312 of FIG. 7 is shown in greater detail. This block 312 operates in three different modes: reservation mode, data transfer mode, and idle mode. The transmit block 312 includes four sixteen bit wide latches 400, 402, 404 and 406. The outputs of each of these latches are controlled by an output enable (OE) input for each latch. The OE of latches 400 and 404 are enabled simultaneously by the transmit line 322. Similarly, the OE of latches 402 and 406 are enabled simultaneously by the output of a logic NAND gate 410 with two inputs: reserve time line 306 and data to send line 314. Latches 400 and 406 have all inputs grounded to a logic zero. Latch 402 receives its input from the output of a 4:16 line decoder 412 which converts the four bit module address to a one of sixteen line output with the one active line at a logic zero. (This function may be merged with that of decoder 352 if desired by inverting the output of decoder 352). The outputs of latches 400 and 402 form a common bus which is 16 bits wide and drives the enable lines of a bank 418 of 16 trapezoidal drivers in the preferred embodiment. A bank 416 of pull-up resistors are coupled to the bus driving the bank 418 of driver's enable lines. The signal inputs of the trapezoidal drivers is provided by the combined outputs of latches 404 and 406. The output of the trapezoidal drivers form the data/reservation bus 54.

Detailed Description Text - DETX (48):

In the idle mode of operation, none of latches 400, 402, 404 and 406 are enabled.